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AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A memory modeling circuit with fault toleration, comprising:

a compare circuit, used to ~~comparing~~ compare memory data stored in the same address in ~~of~~ a plurality of memories, wherein the compare circuit compares at least three data inputs from different memories, wherein if the data inputs are divided into a first kind data and a second kind data and if the count of the first kind data outnumbers that of the second kind data, the compare circuit will output the first kind data; and

a control circuit coupled to said plurality of memories, wherein said control circuit controls said memory data to be read or written from/to said plurality of memories.

2. (Currently Amended) The memory modeling circuit according to claim 1, further comprising:

a test circuit, receiving said memory data and the first kind ~~reading~~ data generated by said compare circuit to generate a testing result.

3. (Currently Amended) The memory modeling circuit according to claim 2, wherein said test circuit further comprises a plurality of sub-test circuits with the same circuit design.

4. (Currently Amended) The memory modeling circuit according to claim 3, wherein said testing result gets an error code and then a faulty memory or a faulty sub-test circuit can be identified according to said error code.

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5. (Currently Amended) The memory modeling circuit according to claim 1, wherein said plurality of memories are the same type of memory.

6. (Currently Amended) The memory modeling circuit according to claim 5, wherein said memory is synchronous dynamic random access memory (SDRAM).

7. (Currently Amended) The memory modeling circuit according to claim 1, wherein said compare circuit further comprises a plurality of sub-compare circuits with the same circuit design.

8. (Currently Amended) The memory modeling circuit according to claim 1, wherein said control circuit is unable to receive ~~stops receiving~~ the first kind data sent from said compare circuit ~~until said control circuit enters the reading mode~~ while said control circuit is in the writing mode.

9. (Currently Amended) The memory modeling circuit according to claim 1, wherein said control circuit is able to receive the first kind data from ~~makes~~ said compare circuit and is unable to receive said memory data from ~~stop writing the data to~~ said plurality of memories ~~until said control circuit enters the writing mode~~ while said control circuit is in the reading mode.

10. (Currently Amended) A memory modeling circuit with fault toleration, comprising:

a compare circuit, used to receive ~~receiving~~ memory data stored in the same address in ~~of~~

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a plurality of memories, wherein the compare circuit compares at least three data inputs from different memories, wherein if the data inputs are divided into a first kind data and a second kind data and if the count of the first kind data outnumbers that of the second kind data, the compare circuit will output the first kind data ~~and comparing the data with each other~~;

a control circuit connecting said plurality of memories, wherein said control circuit can ~~enters~~ a writing mode and writes information ~~data~~ to the same address in ~~of~~ said plurality of memories~~, and said control circuit~~ or enters a reading mode to load data ~~generated by~~ from said compare circuit; and

a test circuit receiving the memory data stored in the same address in ~~of~~ said plurality of memories and the first kind data generated by said compare circuit to generate a testing result.

11. (Currently Amended) The memory modeling circuit according to claim 10, wherein said test circuit further comprises a plurality of sub-test circuits with the same circuit design.

12. (Currently Amended) The memory modeling circuit according to claim 11, wherein said testing result can identify a faulty memory or a faulty sub-test circuit.

13. (Currently Amended) The memory modeling circuit according to claim 10, wherein said compare circuit further comprises a plurality of sub-compare circuits with the same circuit design.

14. (Currently Amended) The memory modeling circuit according to claim 10, wherein

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said testing result gets an error code and then an engineer knows the fault part according to different error code combinations and ~~repair~~ repairs said fault part to keep the reliability.

15. (Currently Amended) The memory modeling circuit according to claim 10, wherein said plurality of memories are the same type of memory.

16. (Currently Amended) The memory modeling circuit according to claim 15, wherein said memory is synchronous dynamic random access memory (SDRAM).

17. (Currently Amended) The memory modeling circuit according to claim 10, wherein said control circuit is unable to receive ~~stops receiving~~ the first kind data sent from said compare circuit ~~until said control circuit enters the reading mode~~ while said control circuit is in the writing mode.

18. (Currently Amended) The memory modeling circuit according to claim 10, wherein said control circuit is able to receive the first kind data from ~~makes~~ said compare circuit and is unable to receive said memory data from ~~stop writing data to~~ said plurality of memories ~~until said control circuit enters the writing mode~~ while said control circuit is in the reading mode.

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